

### **REMARKS/ARGUMENTS**

Claims 7-30 are pending in the present application.

This Amendment is in response to the Final Office Action mailed May 18, 2007 to support a Request for Continued Examination (RCE) filed concurrently. In the Final Office Action, the Examiner rejected claims 19-22 under 35 U.S.C. §101; claims 7, 19, and 27 under 35 U.S.C. §102(); and claims 8, 9, 10-14, 22-22, 24-26, and 28-30 under 35 U.S.C. §103(a). Applicant has amended claims 7, 19, 23, and 27. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

#### ***Rejection Under 35 U.S.C. § 101***

In the Final Office Action, the Examiner rejected claims 19-22 under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. While Applicant disagrees with the Examiner's characterization of the claim language, in the interest of expediting prosecution of the application, Applicant has amended claim 19.

Accordingly, Applicant respectfully requests the rejection be withdrawn.

#### ***Rejection Under 35 U.S.C. § 102***

In the Final Office Action, the Examiner rejected claims 7, 19, and 27 under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,421,809 issued to Wuytack et al. ("Wuytack"). Applicant respectfully traverses the rejection and submits that the Examiner has not met the burden of establishing a prima facie case of anticipation.

Wuytack discloses a method for determining a storage bandwidth optimized memory organization of an essentially digital device. The method is part of a design process of the digital device which is under construction (Wuytack, col. 6, lines 63-65). Only the functional representation of the digital device should be known (Wuytack, col. 6, lines 65-66). The method involves an iterative procedure, starting from an initial scheduling of data access instructions (Wuytack, col. 4, lines 35-37). An extended conflict graph is an undirected hyper-graph, comprising of nodes representing said basic groups; binary edges representing data access conflicts between the two basic groups connected by said binary edge (Wuytack, col. 3, lines 30-

33). A selection of an optimized memory organization satisfying at least the constraints depicted by said optimized extended conflict graph, is performed (Wuytack, col. 3, lines 27-29).

Wuytack does not disclose, either expressly or inherently, at least one of: (1) creating a data layout by mapping each data element to a memory location, the memory location mapping to a corresponding hardware resource, and (2) the data layout being used during execution of the sequence of machine-executable instructions to reduce hardware resource conflicts.

Wuytack merely discloses a design process of the digital device which is under construction (Wuytack, col. 6, lines 63-65), not the memory location mapping to a corresponding hardware resource. Since the digital device is under construction, it is not completed and therefore cannot possess a hardware resource. Wuytack emphatically states that “[i]t must be emphasized that the method according to the present invention is part of [a] design process of [a] digital device [which] is under construction.” (Wuytack, col. 6, lines 63-65). Furthermore, Wuytack specifically discloses that only the functional representation of the digital device should be known (Wuytack, col. 6, lines 65-66). Since only the functional representation of the digital device should be known, there cannot be a mapping of each data element to a memory location which maps to a corresponding hardware resource.

In addition, Wuytack merely discloses that the digital device is described by a representation (Wuytack, col. 6, lines 50-51), not actual hardware including a processor capable of executing instructions, a memory, and/or a compiler. Since it is only a representation, the digital device does not exist and is not capable of executing instructions.

Furthermore, Wuytack merely discloses that a selection of an optimized memory organization satisfying at least the constraints depicted by said optimized extended conflict graph, is performed (Wuytack, col. 3, lines 27-29), not the data layout being used during execution of the sequence of machine-executable instructions to reduce hardware resource conflicts. Selection of an optimized memory organization merely refers to designing a memory organization according to the results provided by the conflict graph. This selection is done during the design of the digital device. Since the digital device has not been designed yet, it is not capable of executing the instructions using the data layout.

To anticipate a claim, the reference must teach every element of the claim. “A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or

inherently described, in a single prior art reference.” Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). “The identical invention must be shown in as complete detail as is contained in the...claim.” Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989). Since the Examiner failed to show that Wuytack teaches or discloses any one of the above elements, the rejection under 35 U.S.C. §102 is improper.

Therefore, Applicant believes that independent claims 7, 19, 23, and 27 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejection under 35 U.S.C. §102 be withdrawn.

### ***Rejection Under 35 U.S.C. § 103***

In the Final Office Action, the Examiner rejected claims 23 under 35 U.S.C. §103(a) as being unpatentable over Wuytack; and claims 8, 9, 10-14, 20-22, 24-26, and 28-30 under 35 U.S.C. §103(a) as being unpatentable over Wuytack in view of U.S. Patent No. 5,774,730 issued to Aizikowitz et al. ("Aizikowitz"). Applicant respectfully traverses the rejection and submits that the Examiner has not met the burden of establishing a *prima facie* case of obviousness.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP* §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004). Applicant respectfully submits that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Furthermore, the Supreme Court in *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966), stated: “Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined.” MPEP 2141. In *KSR International Co. vs. Teleflex, Inc.*, 127 S.Ct. 1727 (2007) (Kennedy, J.), the Court explained that “[o]ften, it will be

necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” The Court further required that an explicit analysis for this reason must be made. “[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR 127 S.Ct.* at 1741, quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). In the instant case, Applicant respectfully submits that there are significant differences between the cited references and the claimed invention and there is no apparent reason to combine the known elements in the manner as claimed, and thus no *prima facie* case of obviousness has been established.

1. Claim 23:

Wuytack discloses a method for determining a storage bandwidth optimized memory organization of an essentially digital device as discussed above.

Wuytack , taken alone or in any combination with other references, does not disclose or render obvious, at least one of: (1) a memory having a sequence of machine-executable instructions that access a plurality of data elements in one or more memory locations; (2) an L2 (level 2) cache having a plurality of data banks, each of the one or more memory locations mapping to one of the plurality of data banks; and (3) circuitry capable of: (a) creating a data layout by mapping each data element to a memory location, the memory location mapping to a corresponding hardware resource, and (b) the data layout being used during execution of the sequence of machine-executable instructions to reduce hardware resource conflicts.

As discussed above, Wuytack does not disclose or render obvious elements (1) and (2) as above. Accordingly, a combination of Wuytack with any other references, including official notice and/or inherency, in rejecting claims 23 is improper.

Furthermore, the Examiner merely contends that it would have been obvious . . . to treat L2 cache as the special case of memory bank (Final Office Action, page 9, lines 9-10).

Applicant respectfully disagrees. Wuytack specifically discloses multi-ported, including dual

ported, memory (Wuytack, col. 11, lines 29-31). A dual-ported memory is a special type of memory used in special processor system. It is not used as a L2 cache.

2. Claims 8, 9, 10-14, 20-22, 24-26, and 28-30:

Wuytack is discussed above.

Aizikowitz discloses a method and apparatus for improving colorability of constrained nodes in an interference graph within a computer system. An interference graph is a tool which may be used to assign a limited number of resources to a large number of items that each need one of the resources (Aizikowitz, col. 11, lines 29-31). The method 700 of coloring a node suitably comprises step 644 in Chaitin's approach (Aizikowitz, col. 11, lines 10-13). Each bit vector 810 represents the colors used by any neighbor as a zero (i.e., unavailable), and represents colors unused by neighbors as a one (i.e., available). (Aizikowitz, col. 11, lines 29-31).

Wuytack and Aizikowitz, taken alone or in any combination, do not disclose or render obvious, at least one of: (1) creating a data layout by mapping each data element to a memory location, the memory location mapping to a corresponding hardware resource, (2) the data layout being used during execution of the sequence of machine-executable instructions to reduce hardware resource conflicts, as recited in claims 7, 19, 23, and 27; and (3) said assigning a color to each of the plurality of nodes comprises, for a given node of each of the plurality of nodes, assigning a color from a corresponding color set, the corresponding color set comprising at least one color from a community color set having a plurality of colors, the at least one color not being in one or more other color sets, the one or more other color sets corresponding to one or more nodes adjacent to the given node, as recited in claims 8, 20, 24, and 28; and (4) other elements as recited in the remaining dependent claims.

As discussed above, Wuytack does not disclose or render obvious elements (1) and (2) as above. Accordingly, a combination of Wuytack with any other references, including official notice and/or inherency, in rejecting claims 8, 9, 10-14, 20-22, 24-26, and 28-30, which depend on claims 7, 19, 23, and 27, respectively is improper.

Furthermore, Aizikowitz merely discloses coloring an interference graph which is a tool used to assign a limited number of resources to a large number of items that each need one of the resources (Aizikowitz, col. 11, lines 29-31), not a conflict graph. The interference graph is not associated with a sequence of machine-executable instructions.

Moreover, Aizikowitz using Chaitin's approach may lead to removing a node or edge if there is spilling (Aizikowitz, col. 7, lines 15-20; col. 11, lines 37-40). The graph, therefore, may be modified, resulting in discrepancy with the sequence of machine-executable instruction. Since modifying Wuytack to incorporate the teachings of Aizikowitz may lead to unsatisfactory result for its intended purposes, there is no suggestion or motivation to make the proposed modification. If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). If the proposed modification or combination of the prior art would change the principle of operation of the prior invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

The Examiner failed to establish the factual inquiries in the three-pronged test as required by the *Graham* factual inquiries. There are significant differences between the cited references and the claimed invention as discussed above. Furthermore, the Examiner has not made an explicit analysis on the apparent reason to combine the known elements in the fashion in the claimed invention. Accordingly, there is no apparent reason to combine the teachings of Wuytack and Aizikowitz.

In the present invention, the cited references do not expressly or implicitly disclose any of the above elements. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Wuytack and Aizikowitz is an obvious application of data layout mechanism to reduce hardware resource conflicts, or an explicit analysis on the apparent reason to combine Wuytack and Aizikowitz in the manner as claimed.

Therefore, Applicant believes that independent claims 7, 19, 23, and 27 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejection under 35 U.S.C. §103(a) be withdrawn.

***Conclusion***

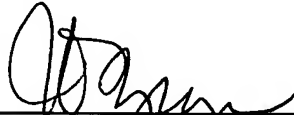
Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 18, 2007

By



Thinh V. Nguyen

Reg. No. 42,034

Tel.: (714) 557-3800 (Pacific Coast)

12400 Wilshire Boulevard, Seventh Floor  
Los Angeles, California 90025

---

**CERTIFICATE OF MAILING/TRANSMISSION (37 CFR 1.8A)**

*I hereby certify that this correspondence is, on the date shown below, being:*

**MAILING**

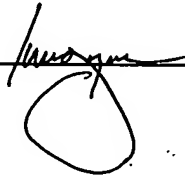
☒ deposited with the United States Postal Service  
as first class mail in an envelope addressed to:  
Commissioner for Patents, PO Box 1450,  
Alexandria, VA 22313-1450.

Date: September 18, 2007

**FACSIMILE**

☐ transmitted by facsimile to the United States Patent  
and Trademark Office.

Tu Nguyen



September 18, 2007

Date